Hi-Flex AMIBIOS

with Writeback Caching and
82C721 Universal Peripheral Support

for Rev B of the

OPTi 82C495

386 SX Chipset

User's Guide

based on the 11/11/92 core AMIBIOS

Use with AMIBCP Version 2.1a

MANOPSX495721
1/27/93

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Revision History

1/27/93 Added 82C721 support and updated to 11/11/92 core AMIBIOS.

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Preface

To the OEM Reader

The Hi-Flex AMIBIOS is a state of the art product which includes major engineering innovations. The Hi-Flex AMIBIOS can be easily configured by the OEM, system integrator, or VAR building systems that include the AMIBIOS through the AMIBIOS Configuration Program (AMIBCP). See the *AMIBCP User's Guide* for detailed information. This manual was written for the OEM to assist in the proper use of AMIBIOS Setup. This manual is not meant to be read by the computer owner who purchases a computer with the AMIBIOS. It is assumed that the computer manufacturer will use this manual as a sourcebook of information, and that parts of this manual will be included in the computer owner's manual. It is also assumed that the OEM, VAR, or system integrator that is reading this manual has also licensed the right to use the AMIBIOS technical documentation.

Technical Support

If an AMIBIOS fails to operate as described or you need more information, call technical support at 404-246-8600. Make sure you have the following information before calling:

- Serial number and revision number of the BIOS
- System BIOS reference number
- A clear description of the problem.

Acknowledgments

This manual was written and edited by Paul Narushoff and Robert Cheng. The writers gratefully acknowledge the assistance of the BIOS engineers.

BIOS File

This manual documents AMIBIOS file OPWB4BP.ROM.

Chapter 1

Introduction

Overview

This manual documents the AMIBIOS for Rev B of the OPTi 82C495 386SX Chipset with write-back caching and C&T 82C721 Universal Peripheral support. This chipset supports systems with Intel 80386SX microprocessor. Please see the OPTi technical documentation for additional information.

OPTi 82C495 Chipset Features

- supports CPUs operating at speeds of from 16 MHz to 33 MHz,
- supports write-back cache memory sizes of 32 KB, 64 KB, 128 KB, 256K, and 512 KB,
- supports up to 16 MB of onboard system RAM in various combinations of 256 KB x 9, 1 MB x 9, and 4 MB x 9 SIMMs (Single Inline Memory Modules).

System BIOS

The BIOS is the basic input output system used in all IBM® PC-, XT™-, AT®-, and PS/2®- compatible computers. The Hi-Flex AMIBIOS is a high-quality example of a system BIOS.

Configuration Data

AT-Compatible systems, also called ISA (Industry Standard Architecture) systems, and EISA (Extended Industry Standard Architecture) systems must have a place to store system information when the computer is turned off. The original IBM AT had 64 bytes of non-volatile memory storage in CMOS RAM. All AT-Compatible systems have at least 64 bytes of CMOS RAM, which is usually part of the Real Time Clock. Many systems have 128 bytes of CMOS RAM.

How Data Is Configured

The AMIBIOS provides a Setup utility in ROM that is accessed by pressing <Del> at the appropriate time during system boot. Setup is used to set configuration data in CMOS RAM.

Types of Setup

Types of Setup	Description
STANDARD CMOS SETUP	Sets time, date, hard disk type, types of floppy drives, monitor type, and if keyboard is installed. These options are documented in the *Hi-Flex AMIBIOS User's Guide*.
ADVANCED CMOS SETUP	Sets Typematic Rate and Delay, Above 1 MB Memory Test, Memory Test Tick Sound, Hit <Del> Message Display, System Boot Up Sequence, and many others. These options are documented in the *Hi-Flex AMIBIOS User's Guide*.
ADVANCED CHIPSET SETUP	Sets chipset-specific options and features. The ADVANCED CHIPSET SETUP options for the AMIBIOS for the OPTi 82C495 386SX chipset are documented on pages through .
Peripheral Setup	Controls Universal Peripheral-related options. See pages through .
Power Management Setup	Controls power conservation options. Not supplied in this BIOS.

Reference

STANDARD CMOS SETUP and the common ADVANCED CMOS SETUP options are described in the *Hi-Flex AMIBIOS User's Guide*. ADVANCED CHIPSET SETUP is described in this manual.

ADVANCED BIOS Features

The ROM file for this BIOS enables Clock Switching and Cache Control via chipset registers.

It does not use the Turbo Switch Input Pin or Reset Memory Controller AMIBCP options.

BIOS Information

The following graphic shows the AMIBCP BIOS Information.

BIOS Options

The following graphic illustrates the AMIBCP BIOS Options for this AMIBIOS file.

Miscellaneous BIOS Features

The following screen shows the AMIBCP Miscellaneous options for this BIOS file.

Chapter 2

ADVANCED CMOS SETUP

Default Settings

Every option in AMIBIOS Setup contains two default values: a power-on default and the BIOS Setup default value.

The Power-on Defaults

The power-on default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

Setup Defaults

The BIOS Setup default values provide optimum performance settings for all devices and system features.

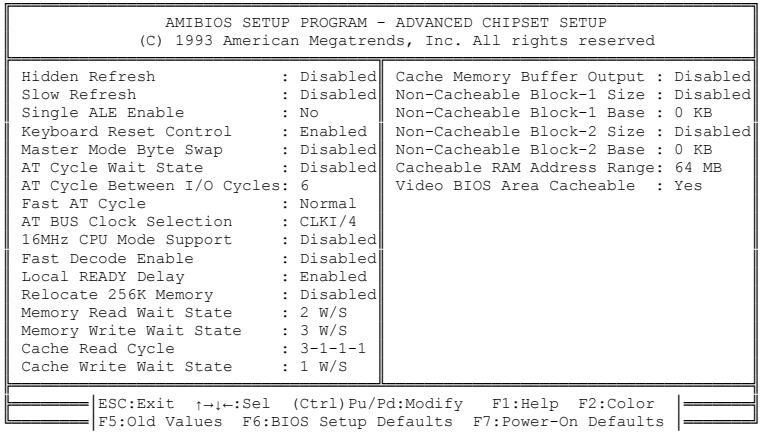
ADVANCED CMOS SETUP Options

The ADVANCED CMOS SETUP options are the same as the standard AMIBIOS ADVANCED CMOS SETUP options documented in the *Hi-Flex AMIBIOS User's Guide*.

Chapter 3

ADVANCED CHIPSET SETUP

Refer to the documentation provided by OPTi for additional assistance in understanding specific options.



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Configuring ADVANCED CHIPSET SETUP Options

You can choose the options that are included in the ADVANCED CHIPSET SETUP via AMIBCP. See the *AMIBCP User's Guide* for additional information.

ADVANCED CHIPSET SETUP Options

Hidden Refresh

If this option is enabled, memory will be refreshed without holding the CPU. This improves system performance. This option should be disabled on 80386-based systems when memory caching support is disabled. The settings are *Enabled* or *Disabled*. The BIOS and Power-on defaults are *Disabled*.

Slow Refresh

Slow Refresh is four times slower (about 64 µseconds) than the normal refresh (about 15.8 µseconds). If enabled, system performance will improve. The settings are *Enabled* or *Disabled*. The BIOS and Power-on defaults are *Disabled*.

Single ALE Enable

If this option is enabled, SYNC will activate Single ALE instead of multiple ALEs during the bus conversion cycle. The settings are *Yes* or *No*. The BIOS and Power-On defaults are *No*.

Keyboard Reset Control

If enabled, a HALT instruction is executed before SYNC generates a CPU reset from a keyboard reset. The BIOS and Power-On default is *Disabled*.

Master Mode Byte Swap

The settings are *Enabled* or *Disabled*. The BIOS and Power-on defaults for this option are *Disabled*.

AT Cycle Wait State

This option adds an additional wait state in the standard AT Bus cycle. The settings are *Enabled* or *Disabled*. The BIOS and Power-on defaults are *Disabled*.

AT Cycle Between I/O Cycles

This option is only valid if Rev B of the chipset is used. The settings are *6* or *2.* The BIOS Setup and Power-On default is *6.*

Fast AT Cycle

This option is only valid if Rev B of the chipset is used. The settings are *Normal* or *Enabled.* The BIOS Setup and Power-On default is *Normal.*

AT BUS Clock Selection

The settings are *CLKI/6, CLKI/4, CLKI/3*, or *CLKI/2.5*. The BIOS and Power-on defaults are *CLKI/4*.

16 MHz CPU Mode Support

This option is only valid if Rev B of the chipset is used. When enabled, the BIOS supports a CPU operating at 16 MHz. When enabled, the AT Bus Clock is set to CLK2I/4. If Disabled is set, the AT Bus Clock is set to the value set in the **AT BUS Clock Selection** option. The settings are *Enabled* or *Disabled.* The BIOS Setup and Power-On default is *Disabled.*

Fast Decode Enable

The settings are *Enabled* or *Disabled*. The BIOS and Power-On defaults are *Disabled*.

Local READY Delay

This option is only valid if Rev B of the chipset is used. When enabled, the BIOS inserts a delay to generate RDY# output. If *Disabled,* RDY# output is not generated. The settings are *Enabled* or *Disabled.* The BIOS Setup and Power-On default is *Enabled.*

Relocate 256K Memory

256 KB x 9 SIMMs must be used in Banks 0 and 1 or in Banks 0, 1, and 2 before this option is valid. When enabled, the 256 KB of memory from A0000h - DFFFFh is relocated to the top of memory. The settings are *Enabled* or *Disabled.* The BIOS Setup and Power-On default is *Disabled.*

Memory Read Wait State

This option sets the number of wait states inserted before DRAM read operations. The settings are *0 W/S, 1 W/S*, or *2 W/S*. The BIOS and Power-on defaults are *2 W/S*.

Memory Write Wait State

This option sets the number of wait states inserted before DRAM write operations. The settings are *0 W/S, 1 W/S, 2 W/S*, or *3 W/S*. The BIOS and Power-on defaults are *3 W/S*.

Cache Read Cycle

This option is only valid if Rev B of the chipset is used. The only current setting is *3-1-1-1*. The BIOS Setup and Power-On default is *3-1-1-1*. If set to 3-2-2-2 or 2-2-2-2, the **Cache Memory Buffer Output** option must be set to *Disabled*.

Cache Write Wait State

This option sets the number of wait states inserted before cache memory write operations. The settings are *0 W/S* or *1 W/S*. The BIOS and Power-on defaults are *1 W/S*.

Cache Memory Buffer Output

This option is only valid if Rev B of the chipset is used. The settings are *Enabled* or *Disabled*. The BIOS and Power-On default is *Disabled*.

Non-Cacheable Block-1 Size
Non-Cacheable Block-2 Size

These options define the size of a region of memory (Block-1 and/or Block-2) in which cache is disabled. The settings for are *64 KB, 128 KB, 256 KB, 512 KB,* or *Disabled*. The BIOS and Power-on defaults are *Disabled.*

Non-Cacheable Block-1 Base
Non-Cacheable Block-2 Base

These options define the base address or starting point of a region of memory in which cache is disabled. The base address changes in increments equal to the corresponding **Non-Cacheable Block-*x* Size**. If the setting of the **Non-Cacheable Block-*x* Size** option is *Disabled,* the only choice for the base address for that block is *0 KB.* The BIOS and Power-on defaults are *0 KB*.

Cacheable RAM Address Range

This option sets the amount of system memory that can be cached. The setting cannot be greater than the total amount of system RAM. The settings are *4 MB, 8 MB, 12 MB, 16 MB, 20 MB, 24 MB, 28 MB, 32 MB, 36 MB, 40 MB, 44 MB, 48 MB, 52 MB, 56 MB, 60 MB*, or *64 MB*.

Video BIOS Area Cacheable

If enabled, the video BIOS shadow RAM area can be cached, which enhances video performance. This option may be enabled only when *Video BIOS Shadowing* is enabled in ADVANCED CMOS SETUP. Before enabling this option (selecting *Yes*), you must be reasonably certain that no application will write to the video BIOS memory area while this option is enabled. The settings are *Yes* or *No*. The BIOS and Power-on defaults are *No*.

Chapter 4

Peripheral Setup

The following screen shows the Peripheral Setup screen displayed for C&T 82C721 Universal Peripheral support.

Programming Option

The settings are *Auto* or *Manual.* When set to *Auto,* the BIOS automatically detects all adapter cards installed in the system and configures the onboard I/O (serial ports, parallel ports, floppy controllers, and IDE controller) automatically. All other Peripheral Setup option settings are ignored. Any serial port, parallel port, floppy controller, or IDE (Integrated Drive Electronics) controller on an adapter card in an expansion slot is configured before onboard I/O. If *Auto* is selected, the BIOS also attempts to avoid IRQ conflicts.

If the offboard serial ports are configured to specific starting I/O ports via jumper settings, the BIOS will configure the onboard serial ports to avoid conflicts. For example, if the default serial port starting I/O ports (serial port1 - 3F8h, serial port2 - 2F8h, serial port3 - 3E8h, serial port4 - 2E8h) are used, the following serial port configurations are possible:

If there are...	**the ports are configured as...**	**and the two onboard serial ports are configured as...**
two offboard serial ports	3E8h and 2F8h	3E8h and 2E8h
two offboard serial ports	3F8h and 3E8h	3F8h and Disabled
one offboard serial port	2F8h	3F8h and Disabled
one offboard serial port	3F8h	2F8h and Disabled

If *Manual* is selected, the settings chosen by the end user in Peripheral Setup apply.

The AMIBIOS reports any I/O conflicts after displaying the BIOS Configuration Summary Screen, but only if *Manual* is chosen. The BIOS and Power-On default is *Auto. The Power-On default must not be changed when running AMIBCP.*

On-Board Floppy Drive

This option enables the use of the floppy drive controller on the motherboard (if installed). The settings are *Enabled* or *Disabled.* The BIOS and Power-On defaults are *Disabled. The Power-On default must not be changed when running AMIBCP.*

On-Board IDE Drive

This option enables the use of the IDE controller on the motherboard (if installed). The settings are *Enabled* or *Disabled.* The BIOS and Power-On defaults are *Disabled. The Power-On default must not be changed when running AMIBCP.*

First Serial Port Address

This option enables serial port 1 on the motherboard (if installed). The BIOS and Power-On defaults are *Disabled.* The settings are *Disabled* or any valid I/O port address consisting of three hex digits. The settings are taken from the I/O ports for serial port1 entered in the AMIBCP *Configure Miscellaneous Options* Screen. *The Power-On default must not be changed when running AMIBCP.*

Second Serial Port Address

This option enables serial port 2 on the motherboard, if installed. The BIOS and Power-On defaults are *Disabled.* The settings are *Disabled* or any valid I/O port address consisting of three hex digits. The settings are taken from the I/O ports for serial port2 entered in the AMIBCP *Configure Miscellaneous Options* Screen. *The Power-On default must not be changed when running AMIBCP.*

Parallel Port Address

This option enables the parallel port on the motherboard, if installed. The settings are *Disabled* or any valid I/O port address consisting of three hex digits. The BIOS and Power-On defaults are *Disabled. The Power-On default must not be changed when running AMIBCP.*

IRQ Active State

The settings are *High* or *Low.* The BIOS and Power-On default is *High.*

Parallel Port Mode

The settings are *Extended* or *Normal.* The extended parallel port mode is bidirectional. The BIOS and Power-On default is Normal.

Chapter 5

CMOS Map

A map of CMOS RAM as configured by the AMIBIOS for Rev B of the OPTi 82C495 386SX chipset with 82C721 support is shown in the following table.

Offset	Description
00h - 0Fh	Standard IBM AT compatible RTC and Status Register data definitions.
10h	Floppy Drive Type Bits 7-4 Drive A: Type 0 No Drive 1 360 KB Drive 2 1.2 MB Drive 3 720 KB Drive 4 1.44 MB Drive 5-16 Reserved Bits 3-0 Drive B: Type (bit settings same as A)
11h	Keyboard Typematic Data Bit 7 Typematic Rate Programming (1 = On) Bits 6-5 Typematic Delay 00b 250 ms 01b 500 ms 10b 750 ms 11b 100 ms Bits 4-0 Typematic Rate 0 6 1 6 2 10 3 12 4 15 5 20 6 24 7 30
12h	Hard Disk Data Bits 7-4 Hard Disk Drive C: Type 0 No drive 1-14 Hard drive Type 1-14 16 Hard Disk Type 16-255 (actual Hard Drive Type is in CMOS RAM 1Ah) Bits 3-0 Hard Disk Drive D: Type (Same as C:)
13h	Bit 7 Mouse Support Option (1 = On) Bit 6 Above 1 MB Memory Test (1 = On) Bit 5 Memory Test Tick Sound (1 = On) Bit 4 Memory Parity Error Check (1 = On) Bit 3 Hit <DEL> Message Display (1 = On) Bit 2 Hard Disk Type 47 RAM Area (1 = 0:300h) Bit 1 Wait for <F1> if Any Error (1 = On) Bit 0 Num Lock Enable (1 = On)
14h	Equipment Byte Bits 7-6 Number of Floppy Drives 00b 1 Drive 01b 2 Drives 10b-11b Reserved

	Bits 5-4 Monitor Type 00b Not CGA or MDA 01b 40x25 CGA 10b 80x25 CGA 11b MDA (Monochrome) Bit 3 Display Enabled (1 = On) Bit 2 Keyboard Enabled (1 = On) Bit 1 Math coprocessor Installed (1 = On) Bit 0 Floppy Drive Installed (0 = On)
15h	Base Memory (in 1K increments), Low Byte
16h	Base Memory (in 1K increments), High Byte
17h	Extended Memory (in 1K increments), Low Byte
18h	Extended Memory (in 1K increments), High Byte (Max 15 MB)
19h	Hard Disk C: Drive Type 0-15 Reserved 16-255 Hard Drive Type 16-255
1Ah	Hard Disk D: Drive Type (Same as Drive C: above)
1Bh	User-Defined Drive C: - # of Cylinders, Low Byte
1Ch	User-Defined Drive C: - # of Cylinders, High Byte
1Dh	User-Defined Drive C: - Number of Heads
1Eh	User-Defined Drive C: - Write Precompensation Cylinder, Low Byte
1Fh	User-Defined Drive C: - Write Precompensation Cylinder, High Byte
20h	User-Defined Drive C: - Control Byte (80h if # of heads is equal or greater than 8)
21h	User-Defined Drive C: - Landing Zone, Low Byte
22h	User-Defined Drive C: - Landing Zone, High Byte
23h	User-Defined Drive C: - # of Sectors
24h	User-Defined Drive D: - # of Cylinders, Low Byte
25h	User-Defined Drive D: - # of Cylinders, High Byte
26h	User-Defined Drive D: - Number of Heads
27h	User-Defined Drive D: - Write Precompensation Cylinder, Low Byte
28h	User-Defined Drive D: - Write Precompensation Cylinder, High Byte
29h	User-Defined Drive D: - Control Byte (80h if # of heads is equal or greater than 8)
2Ah	User-Defined Drive D: - Landing Zone, Low Byte
2Bh	User-Defined Drive D: - Landing Zone, High Byte
2Ch	User-Defined Drive D: - # of Sectors
2Dh	Configuration Options Bit 7 Weitek Installed (1 = On) Bit 6 Floppy Drive Seek At Boot (1 = On) Bit 5 System Boot Up Sequence (1 = A:, C:) Bit 4 System Boot Up CPU Speed (1 = High) Bit 3 External Cache Memory (1 = On) Bit 2 Internal Cache Memory (1 = On)

	Bit 1 Fast Gate A20 Option (1 = On) Bit 0 Turbo Switch (1 = On)
2Eh	Standard CMOS Checksum, High Byte
2Fh	Standard CMOS Checksum, Low Byte
30h	Extended Memory, Low Byte
31h	Extended Memory, High Byte (Maximum 15 MB)
32h	Century Byte (BCD value for the century)
33h	Information Flag Bit 7 BIOS Size (1 = 128 KB) Bits 6-0 Reserved
34h	Bit 7 Boot Sector Virus Protection (1 = On) Bit 6 Password 0 Always 0 Setup Bit 5 Adaptor ROM Shadow C800,16K (1 = On) Bit 4 Adaptor ROM Shadow CC00,16K (1 = On) Bit 3 Adaptor ROM Shadow D000,16K (1 = On) Bit 2 Adaptor ROM Shadow D400,16K (1 = On) Bit 1 Adaptor ROM Shadow D800,16K (1 = On) Bit 0 Adaptor ROM Shadow DC00,16K (1 = On)
35h	Shadowing Bit 7 Adaptor ROM Shadow E000,16K (1 = On) Bit 6 Adaptor ROM Shadow E400,16K (1 = On) Bit 5 Adaptor ROM Shadow E800,16K (1 = On) Bit 4 Adaptor ROM Shadow EC00,16K (1 = On) Bit 3 System BIOS Shadow F000,64K (1 = On) Bit 2 Video ROM Shadow C000, 16K (1 = On) Bit 1 Video ROM Shadow C400,16K (1 = On) Bit 0 Numeric Coprocessor (1 = On)
36h	Reserved
38h - 3Dh	Encrypted Password
3Eh	Extended CMOS Checksum, High Byte (includes 34h - 3Dh)
3Fh	Extended CMOS Checksum, Low Byte (includes 34h - 3Dh)

Extended CMOS RAM

CMOS Location	Description
40h–5Fh	Reserved
60h	Bits 7–5 Reserved Bit 4 Cache Memory Buffer Output Bit 3 Single ALE Enable Bit 2 AT Cycle Wait State Bit 1 Keyboard Reset Control Bit 0 Reserved
61h	Bit 7 Master Mode Byte Swap Bits 6–2 Reserved Bit 1 Cache Write Wait State Bit 0 Cache Read Cycle
62h	Bits 7–3 Reserved Bit 2 Hidden Refresh Bit 1 Reserved Bit 0 Slow Refresh
63h	Reserved
64h	Bit 3 16MHz CPU Mode Support
65h	Bits 7–6 Memory Read Wait State Bits 5–4 Memory Write Wait State Bit 3 Fast Decode Enable Bits 1-0 AT BUS Clock Selection
66h	Bit 7 Fast AT Cycle
67h	Bit 6 Local READY Delay Bit 5 AT Cycle Between I/O Cycles Bits 4 Video BIOS Area Cacheable Bits 3–0 Cacheable RAM Address Range
68h	Bits 7–5 Non-Cacheable Block-1 Size Bit 3 Relocate 256K Memory
69h	Bits 7-0 Non-Cacheable Block-1 Base
6Ah	Bits 7–5 Non-Cacheable Block-2 Size
6Bh	Bits 7-0 Non-Cacheable Block-2 Base
6Ch	Bit 4 On-board Floppy Drive Bit 0 On-board IDE Drive
6Dh	Bit 4 IRQ Active State Bit 3 Parallel Port Mode Bits 1-0 Parallel Port Address
6Eh	Reserved
6Fh	Bits 7-5 First Serial Port Address Bits 4-2 Second Serial Port Address Bit 0 Programming Option
70h–7Fh	Reserved

Chapter 6

Chipset Registers

The AMIBIOS for the OPTi 82C495 386SX chipset sets the chipset registers as follows.

Register	Description
00h	Bit 4 Onboard Floppy Drive 0 Disabled 1 Enabled Bit 0 Onboard IDE Drive 0 Disabled 1 Enabled
01h	Bit 4 IRQ Active State 0 Low 1 High Bit 3 Parallel Port Mode 0 Extended 1 Normal Bits 1-0 Parallel Port Address
02h	Reserved
03h	Bits 7-5 First Serial Port Address Bits 4-2 Second Serial Port Address Bit 0 Programming Option 0 Auto 1 Manual
20h	Bit 4 Cache Memory Buffer Output 0 Disabled 1 Enabled Bit 3 Single ALE Enable 0 No 1 Yes Bit 2 AT Cycle Wait State 0 Disabled 1 Enabled Bit 1 Keyboard Reset Control 0 Enabled 1 Disabled
21h	Bit 7 Master Mode Byte Swap 0 Disabled 1 Enabled Bits 6 & 1 Cache Write Wait State 00 1 W/S 01 0 W/S 10 2 W/S Bit 0 Cache Read Cycle
22h	Bit 2 Hidden Refresh 0 Enabled 1 Disabled Bit 0 Slow Refresh

	0 1	Enabled Disabled		
23h	Reserved			
24h	Bit 3 0 1	16 MHz CPU Mode Select Disabled Enabled		
25h	Bits 7-6 01 10 11 Bits 5-4 00 01 10 11 Bit 3 0 1 Bits 1-0 00 01 10 11	Memory Read Wait State 0 W/S 1 W/S 2 W/S Memory Write Wait State 0 W/S 1 W/S 2 W/S 3 W/S Fast Decode Enable Disabled Enabled AT BUS Clock Selection CLKI/6 CLKI/4 CLKI/3 CLKI/5		
26h	Bit 7 0 1	Fast AT Cycle Normal Enabled		
27h	Bit 6 0 1 Bit 5 0 1 Bit 4 0 1 Bits 3-0 0000 0010 0100 0110 1000 1010 1100 1110	Local READY Delay Enabled Disabled AT Cycle Between I/O Cycles 6 2 Video BIOS Area Cacheable Yes No Cacheable RAM Address Range 64 MB 8 MB 16 MB 24 MB 32 MB 40 MB 48 MB 56 MB	0001 0011 0101 0111 1001 1011 1101 1111	 4 MB 12 MB 20 MB 28 MB 36 MB 44 MB 52 MB 64 MB
28h	Bits 7-5 000 010	Non-Cacheable Block-1 Size 64 KB 256 KB	001 011	 128 KB 512 KB
29h	Bits 7-0	Non-Cacheable Block-1 Base		
2Ah	Bits 7-5 000 010	Non-Cacheable Block-2 Size 64 KB 256 KB	001 011	 128 KB 512 KB
2Bh	Non-Cacheable Block-2 Base			

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